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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,569	12/14/2001	Judson A. Lehman	US018183	8131

7590 06/24/2004

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EXAMINER	
DAMIANO, ANNE L	

ART UNIT	PAPER NUMBER
2114	4

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/017,569	LEHMAN ET AL.
	Examiner	Art Unit
	Anne L Damiano	2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Parrish (6,631,483)

As in claim 1, Parrish discloses a method for enhancing the security of a system operating in conjunction with a clock signal from a system clock (column 1: lines 45-47) (The system protecting against failure is taking safety measures to increase the stableness or security of the system.), comprising:

Monitoring the system for detecting a fault (loss of signal from clock) in the system (column 2: lines 47-49 and column 10: lines 60-64);

Upon detection of a fault, switching the system from operating in conjunction with a clock signal from the system clock to operate in conjunction with a secure clock signal from a secure clock (column 2: lines 49-58, column 10: line 65-column 11: line22). (The acceptability of secondary reference clock is checked and the switchover is made if the secondary clock is acceptable. The second clock being acceptable means it is a reliable and secure clock.)

As in claim 2, Parrish discloses the method of claim 1, wherein the system is switched to operate in conjunction with a secure clock signal from one of a plurality of secure clocks (column 8: lines 45-57). (The "health" of the candidate reference clock signals is evaluated meaning that if the clocks are considered "healthy," they are reliable and secure.)

As in claim 3, Parrish discloses the method of claim 1, further comprising:

Monitoring the system operating in conjunction with a clock signal from a secure clock,

Upon detecting cessation of said fault in the system (recovery), switching the system to again operate in conjunction with a clock signal from the system clock (column 10: lines 53-59).

As in claim 4, Parrish discloses the method of claim 3, further comprising switching the system back to the clock signal from the system clock even if the system clock is not operating (column 10: line 60-column 13).

As in claim 5, Parrish discloses the method of claim 1 further comprising monitoring the system for detecting a fault associated with one of an over-frequency and under-frequency clock signals from the system clock (column 5: lines 61-65). (Detecting all clock failures includes monitoring for over and under frequency clock signals.)

As in claim 6, Parrish discloses the method of claim 1, further comprising:

When switching the system to operate in conjunction with the secure clock signal from the secure clock, preventing the clock signal from having short transitions that do not cross the logic threshold from a high to low state or a low to high state (column 10 line 65-column 11: line 14). (When switching, the system enters into holdover mode, in which the internal reference clock drives the clock generator, which, in turn, is preventing the clock signal from having short transitions that do not cross the logic threshold from a high to low state or a low to high state.)

As in claim 7, Parrish discloses the method of claim 1, wherein when switching from the clock signal of the system clock to the secure clock signal of the secure clock, the clock signal has an extend low time (column 11: lines 14-24).

As in claim 8, Parrish discloses the method of claim 1 further comprising multiplexing together clock signals from the system clock and from at least one secure clock and, upon detecting a fault, selecting one of the multiplexed clock signals for operating the system (column 9: lines 48-53).

As in claim 9, Parrish discloses the method of claim 3 further comprising, when switching between clock signals, waiting until the clock signal, which is being switched from, transitions to a low state (column 11: lines 14-23).

As in claim 10, Parrish discloses an apparatus for enhancing the security of a system operating in conjunction with a clock signal from a system clock, the apparatus comprising:

A secure clock generating a secure clock signal (column 8: lines 45-57) (The "health" of the candidate reference clock signals is evaluated meaning that if the clocks are considered "healthy," they are reliable and secure.);

A clock monitor circuit configured to monitor the system for detecting a fault (loss of signal from clock) (column 2: lines 47-49 and column 10: lines 60-64);

Clock switching circuitry, the clock switching circuitry operably coupled to the clock monitor circuit, the system clock signal and the secure clock signal (column 2: lines 53-58);

The clock switching circuitry configured, upon the detection of a fault, to switch the system from operating in conjunction with a clock signal from the system clock to operate in conjunction with a secure clock signal from a secure clock (column 2: lines 49-58, column 10: line 65-column 11: line 22). (The acceptability of secondary reference clock is checked and the switchover is made if the secondary clock is acceptable. The second clock being acceptable means it is a reliable and secure clock.)

As in claim 11, Parrish discloses the apparatus of claim 10, further comprising: a plurality of secure clocks with secure clock signals; the clock switching circuitry operably coupled to plurality of secure clock signals for switching the system to operate in conjunction with one of the secure clock signals (column 8: lines 45-57). (The "health" of the candidate reference clock signals is evaluated meaning that if the clocks are considered "healthy," they are reliable and secure.)

As in claim 12, Parrish discloses the apparatus of claim 10, wherein the secure clock includes a ring oscillator (column 6: lines 61-65).

As in claim 13, Parris discloses the apparatus of claim 10, wherein the clock monitor circuit is configured to detect the cessation of the detected fault;

The clock switching circuitry further configured to switch the system to again operate in conjunction with a clock signal from the system clock upon detecting the cessation of said fault (column 10: lines 53-59).

As in claim 14, Parrish discloses the apparatus of claim 10 wherein the clock monitor circuit is configured to monitor the system for detecting a fault associated with one of an over-frequency and under-frequency clock signals from the system clock, the clock switching circuitry configured to switch the system to operate in conjunction with a secure clock signal from a secure clock to prevent over-frequency and under-frequency clocking of the system (column 5: lines 61-65). (Detecting all clock failures includes monitoring for over and under frequency clock signals.)

As in claim 15, Parrish discloses the apparatus of claim 14 wherein the clock monitor circuit includes frequency dividers; and, delay lines, the frequency dividers and delay lines configured to detect over-frequency and under-frequency clock signals from the system clock (column 8: lines 25-27).

As in claim 16, Parrish discloses an application specific integrated circuit (column 7: lines 31-37 and lines 48-56) comprising:

A processor (CPU);

A clock generating a system clock signal for operation of the processor (column 6: lines 31- 42);

The secure clock further generating a secure clock signal (column 8: lines 45-57) (The "health" of the candidate reference clock signals is evaluated meaning that if the clocks are considered "healthy," they are reliable and secure.);

A clock monitor circuit configured to monitor the application specific integrated circuit for detecting a fault (column 2: lines column 8: lines 45-57);

Clock switching circuitry, the clock switching circuitry operably coupled to the clock monitor circuit, the system clock signal and the secure clock signal (column 2: lines 53-58);

The clock switching circuitry configured, upon the detection of a fault, to switch the processor from operating in conjunction with a system clock signal to operating in conjunction with the secure clock signal (column 2: lines 49-58, column 10: line 65-column 11: line 22). (The acceptability of secondary reference clock is checked and the switchover is made if the secondary clock is acceptable. The second clock being acceptable means it is a reliable and secure clock.)

As in claim 17, Parrish discloses the circuit of claim 16, further comprising:

A plurality of secure clocks with secure clock signals;

The clock switching circuitry operably coupled to plurality of secure clock signals for switching the system to operate in conjunction with one of the secure clock signals (column 8: lines 45-57). (The "health" of the candidate reference clock signals is evaluated meaning that if the clocks are considered "healthy," they are reliable and secure.)

As in claim 18, Parrish discloses the circuit of claim 16, wherein the clock monitor circuit is configured to detect the cessation of the detected fault;

The clock switching circuitry further configured to switch the processor to again operate in conjunction with the system clock signal upon detecting the cessation of said fault (recovery) (column 10: lines 53-59).

As in claim 19, Parrish discloses the circuit of claim 16 wherein the clock monitor circuit is configured to monitor the circuit for detecting a fault associated with one of an over-frequency and under-frequency system clock signal, the clock switching circuitry configured to switch the processor to operate in conjunction with a secure clock signal from a secure clock to prevent over-frequency and under-frequency clocking of the processor (column 5: lines 61-65). (Detecting all clock failures includes monitoring for over and under frequency clock signals.)

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD

SCOTT BADERMAN
PRIMARY EXAMINER